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(54) **ORGANIC LIGHT-EMITTING DISPLAY DEVICE**

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(57) **ABSTRACT**

An organic light-emitting diode (OLED) display device includes a substrate, a first gate electrode on the substrate, a second gate electrode on the first gate electrode and at least partially overlapping the first gate electrode, a semiconductor pattern between the first gate electrode and the second gate electrode and at least partially overlapping the first and second gate electrodes, a connecting electrode on the second gate electrode and electrically connected to the semiconductor pattern, and a pixel electrode on the connecting electrode and electrically connected to the connecting electrode.

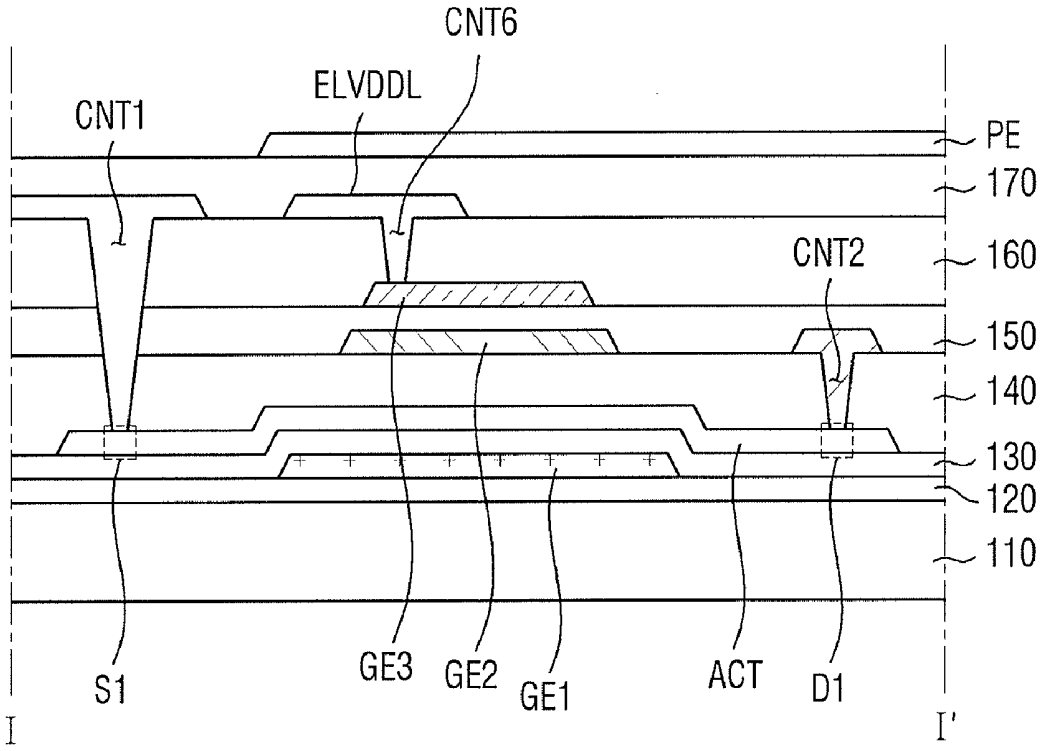


FIG. 1

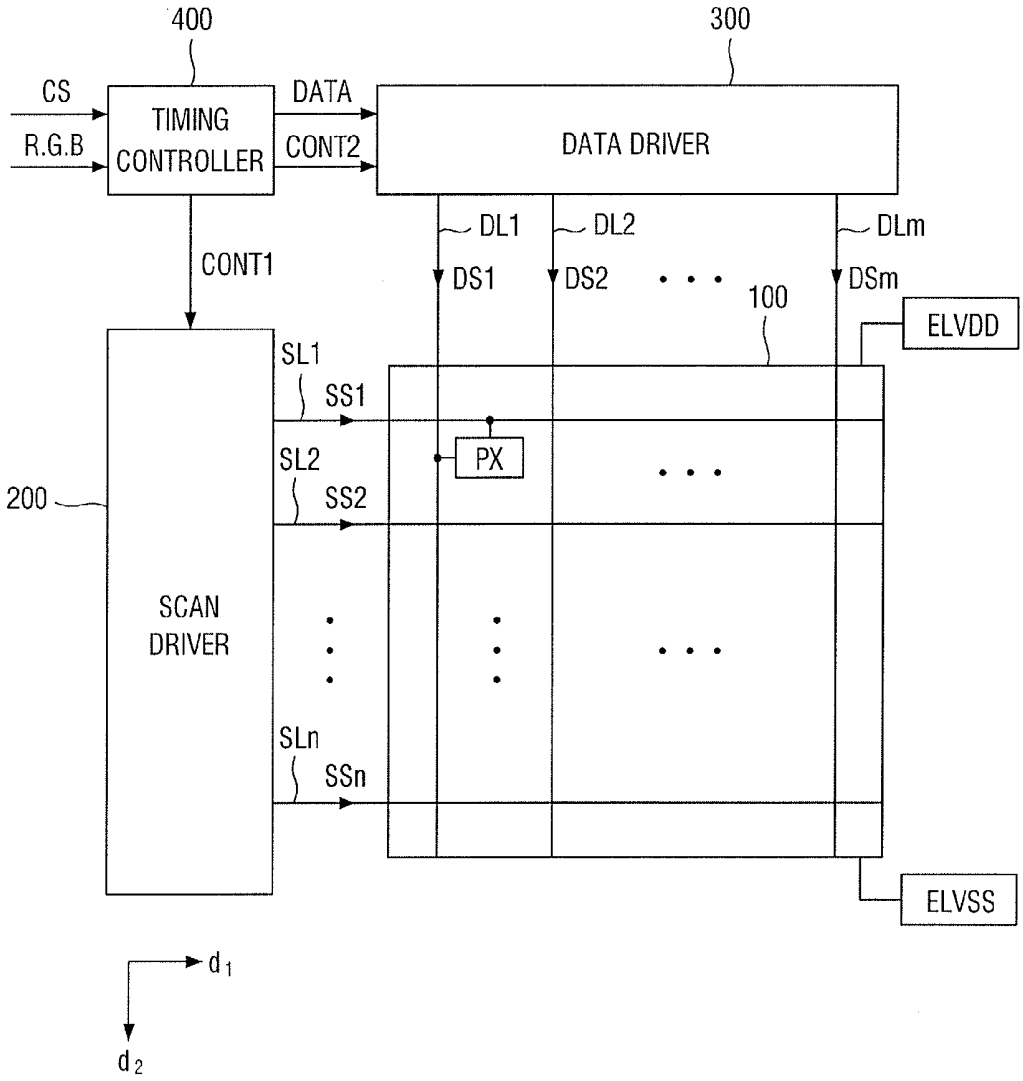

400
300
CS
R.G.B
TIMING CONTROLLER
DATA
CONT2
DATA DRIVER
CONT1
DL1
DL2
DLm
DS1
DS2
DSm
100
ELVDD
SL1
SS1
SL2
SS2
PX
200
SCAN DRIVER
SLn
SSn
ELVSS
d1
d2

FIG. 2

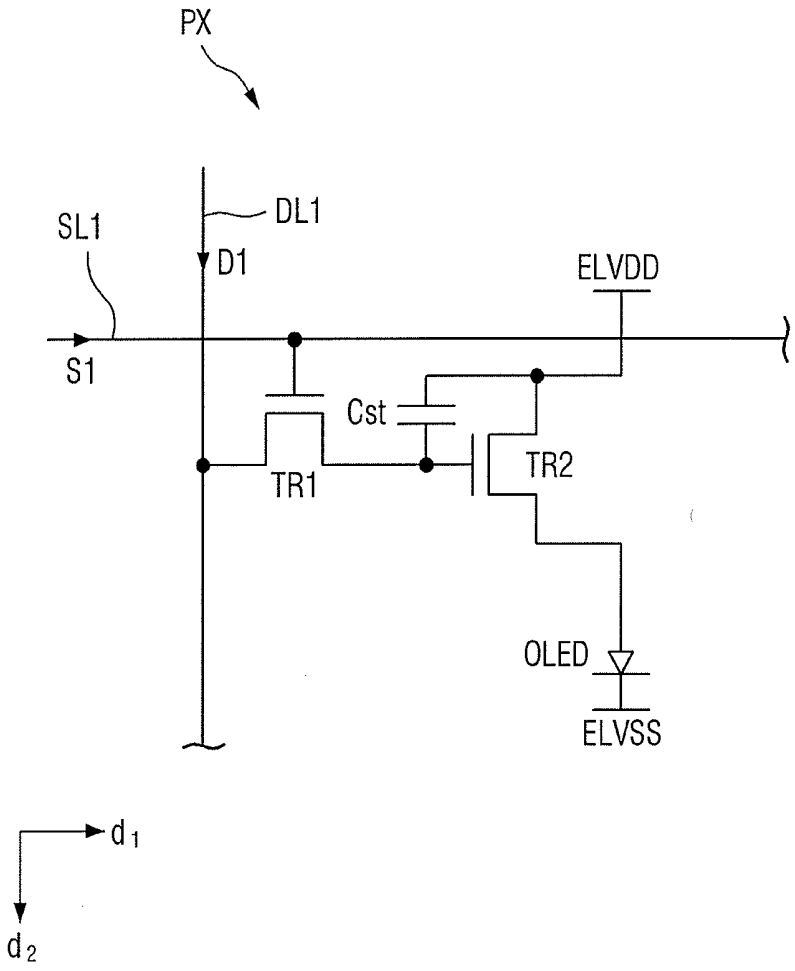


FIG. 3

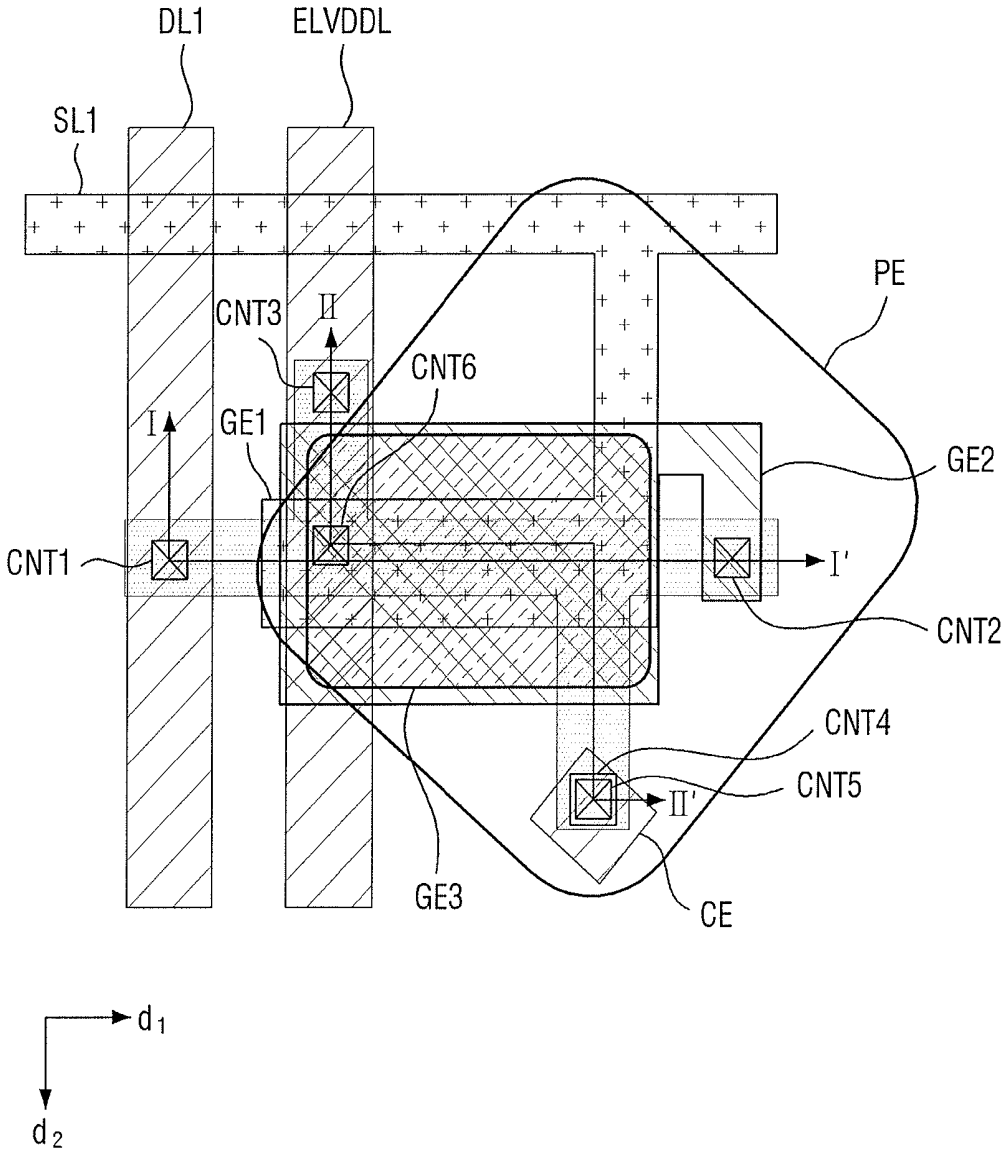

DL1
ELVDDL
SL1
PE
CNT3
II
CNT6
I
GE1
GE2
CNT1
I'
CNT2
CNT4
CNT5
II'
GE3
CE
d1
d2

FIG. 4

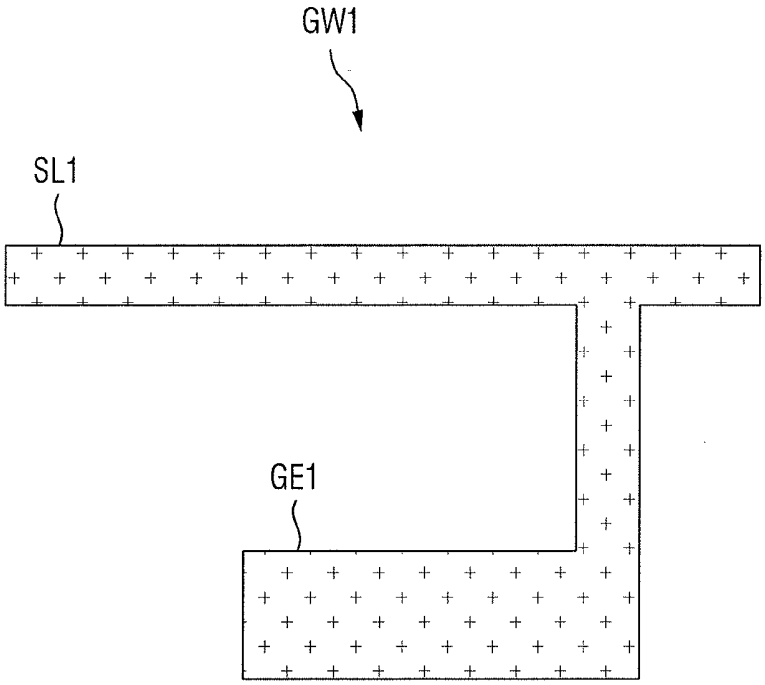


FIG. 5

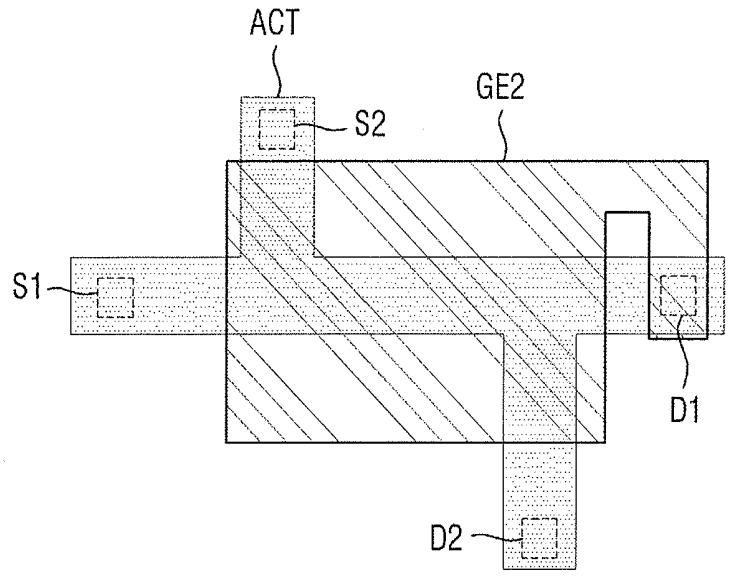


FIG. 6

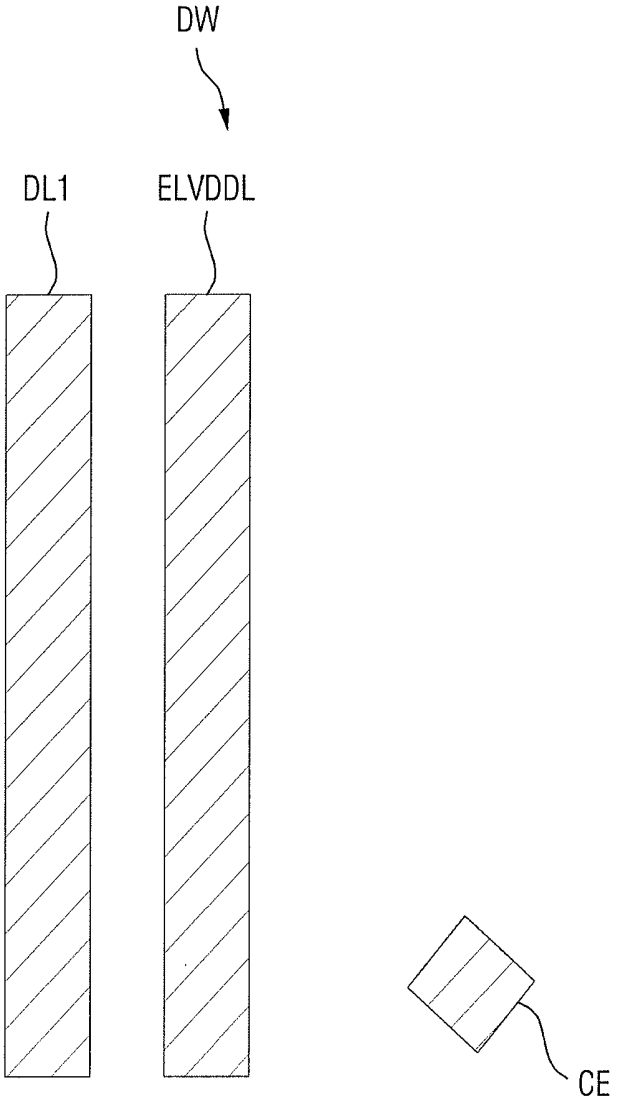


FIG. 7

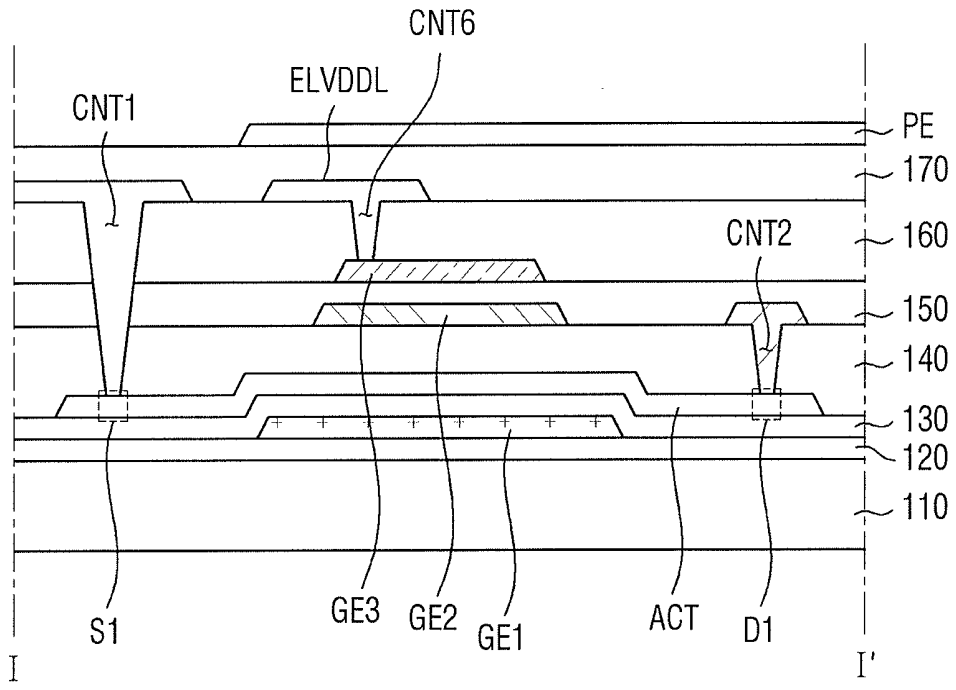
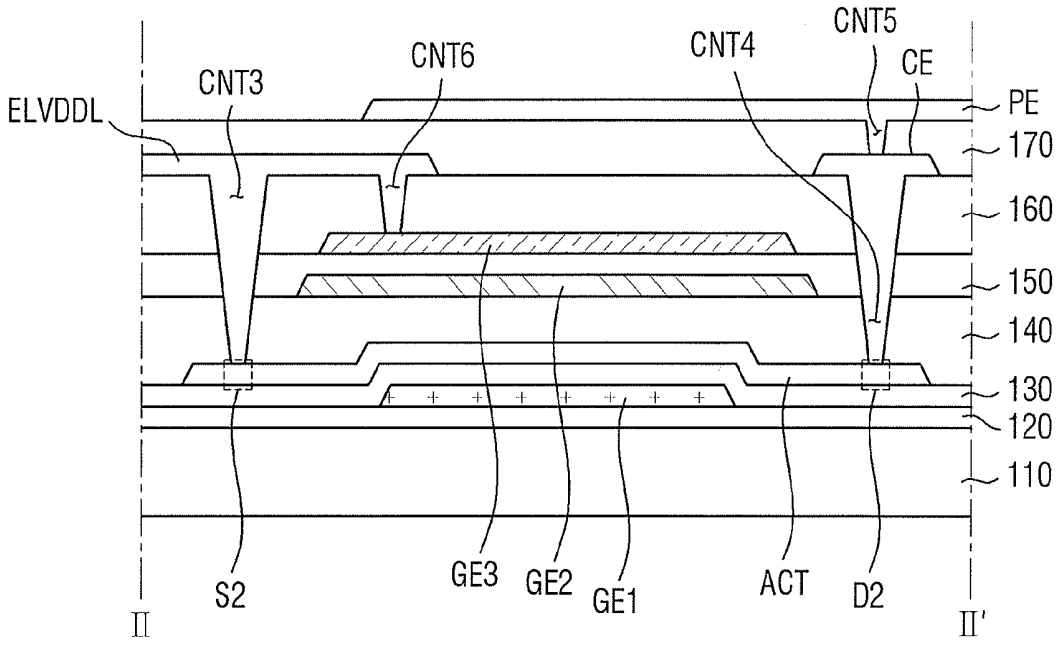

CNT6
ELVDDL
CNT1
PE
170
CNT2
160
150
140
130
120
110
S1
GE3
GE2
GE1
ACT
D1
I
I'

FIG. 8


CNT5
CNT4
CNT6
CE
CNT3
ELVDDL
PE
170
160
150
140
130
120
110
S2
GE3
GE2
GE1
ACT
D2
II
II'

ORGANIC LIGHT-EMITTING DISPLAY DEVICE

CROSS-REFERENCE TO RELATED APPLICATION

[0001] Korean Patent Application No. 10-2016-0133525, filed on Oct. 14, 2016, in the Korean Intellectual Property Office, and entitled: "Organic Light-Emitting Display Device," is incorporated by reference herein in its entirety.

BACKGROUND

1. Field

[0002] Exemplary embodiments relate to an organic light-emitting display device.

2. Description of the Related Art

[0003] Display devices become more and more important as multimedia technology evolves. Accordingly, a variety of types of display devices, e.g., liquid-crystal display (LCD) devices and organic light-emitting diode (OLED) display devices, are currently used.

[0004] For example, the OLED display device displays images by using an organic light-emitting device that emits light as electrons and holes recombine. Such an organic light-emitting display device has advantages in that it has fast response speed, high luminance and large viewing angle, and low power consumption.

SUMMARY

[0005] In an exemplary embodiment, an OLED display includes a substrate, a first gate electrode disposed on the substrate, a second gate electrode disposed on the first gate electrode and at least partially overlapping with the first gate electrode, a semiconductor pattern disposed between the first gate electrode and the second gate electrode and at least partially overlapping with the first and second gate electrodes, a connecting electrode disposed on the second gate electrode and electrically connected to the semiconductor pattern, and a pixel electrode disposed on the connecting electrode and electrically connected to the connecting electrode.

[0006] In another exemplary embodiment, an OLED display device includes a substrate, a first gate electrode disposed on the substrate, a semiconductor pattern disposed on the first gate electrode and including a first source region, a second source region, a first drain region and a second drain region, a second gate electrode disposed on the semiconductor pattern and electrically connected to the first drain region of the semiconductor pattern, a connecting electrode disposed on the second gate electrode and electrically connected to the second drain region of the semiconductor pattern, a data line disposed on the same layer as the connecting electrode and electrically connected to the first source region, and a driving voltage line disposed on the same layer as the data line and electrically connected to the second source region.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] Features will become apparent to those of ordinary skill in the art by describing in detail exemplary embodiments with reference to the attached drawings, in which:

[0008] FIG. **1** illustrates a block diagram of an OLED display device including a stacked device according to an exemplary embodiment of the present disclosure;

[0009] FIG. **2** illustrates an equivalent circuit diagram of the pixel in FIG. **1**;

[0010] FIG. **3** illustrates a schematic layout diagram of the pixel in FIG. **1**;

[0011] FIG. **4** illustrates a first gate conductor of the pixel in FIG. **3**;

[0012] FIG. **5** illustrates a semiconductor pattern and a second gate electrode of the pixel in FIG. **3**.

[0013] FIG. **6** illustrates a data conductor of the pixel in FIG. **3**;

[0014] FIG. **7** illustrates a cross-sectional view along line I-I' in FIG. **3**; and

[0015] FIG. **8** illustrates a cross-sectional view along line II-II' in FIG. **3**.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0016] Example embodiments will now be described more fully hereinafter with reference to the accompanying drawings; however, they may be embodied in different forms and should not be construed as limited to the embodiments set forth herein. Rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey exemplary implementations to those skilled in the art.

[0017] In the drawing figures, the dimensions of layers and regions may be exaggerated for clarity of illustration. It will also be understood that when an element or layer is referred to as being "on," "connected to," or "coupled to" another element or layer, it may be directly on, connected to, or coupled to the other element or layer or intervening elements or layers may be present. When, however, an element or layer is referred to as being "directly on," "directly connected to," or "directly coupled to" another element or layer, there are no intervening elements or layers present. For the purposes of this disclosure, "at least one of X, Y, and Z" and "at least one selected from X, Y, and Z" may be construed as X only, Y only, Z only, or any combination of two or more of X, Y, and Z, such as, for instance, XYZ, XYY, YZ, and ZZ. Like reference numerals refer to like elements throughout.

[0018] Although the terms first, second, etc. may be used herein to describe various elements, components, regions, layers, and/or sections, these elements, components, regions, layers, and/or sections should not be limited by these terms. These terms are used to distinguish one element, component, region, layer, and/or section from another element, component, region, layer, and/or section. Thus, a first element, component, region, layer, and/or section discussed below could be termed a second element, component, region, layer, and/or section without departing from the teachings of the disclosure.

[0019] Spatially relative terms, such as "beneath," "below," "lower," "above," "upper," and the like, may be used herein for descriptive purposes, and, thereby, to describe one element or feature's relationship to another element(s) or feature(s) as illustrated in the drawings. Spatially relative terms are intended to encompass different orientations of an apparatus in use, operation, and/or manufacture in addition to the orientation depicted in the drawings. For example, if the apparatus in the drawings is turned

over, elements described as "below" or "beneath" other elements or features would then be oriented "above" the other elements or features. Thus, the exemplary term "below" can encompass both an orientation of above and below. Furthermore, the apparatus may be otherwise oriented (e.g., rotated **90** degrees or at other orientations), and, as such, the spatially relative descriptors used herein interpreted accordingly.

[0020] The terminology used herein is for the purpose of describing particular embodiments and is not intended to be limiting. As used herein, the singular forms, "a," "an," and "the" are intended to include the plural forms as well, unless the context clearly indicates otherwise. "Or" means "and/or." As used herein, the term "and/or" includes any and all combinations of one or more of the associated listed items. It will be further understood that the terms "comprises," "comprising," "includes," and/or "including," when used in this specification, specify the presence of stated features, integers, steps, operations, elements, components, and/or groups thereof, but do not preclude the presence or addition of one or more other features, integers, steps, operations, elements, components, and/or groups thereof.

[0021] "About" or "approximately" as used herein is inclusive of the stated value and means within an acceptable range of deviation for the particular value as determined by one of ordinary skill in the art, considering the measurement in question and the error associated with measurement of the particular quantity (i.e., the limitations of the measurement system). For example, "about" can mean within one or more standard deviations, or within ±30%, 20%, 10%, 5% of the stated value.

[0022] Various exemplary embodiments are described herein with reference to sectional illustrations that are schematic illustrations of idealized exemplary embodiments and/or intermediate structures. As such, variations from the shapes of the illustrations as a result, for example, of manufacturing techniques and/or tolerances, are to be expected, e.g., a region illustrated or described as flat may have rough and/or nonlinear features, or sharp angles may be illustrated as rounded. Thus, exemplary embodiments disclosed herein should not be construed as limited to the particular illustrated shapes of regions, but are to include deviations in shapes that result from, for instance, manufacturing.

[0023] Unless otherwise defined, all terms (including technical and scientific terms) used herein have the same meaning as commonly understood by one of ordinary skill in the art. Terms, such as those defined in commonly used dictionaries, should be interpreted as having a meaning that is consistent with their meaning in the context of the relevant art and will not be interpreted in an idealized or overly formal sense, unless expressly so defined herein.

[0024] Hereinafter, exemplary embodiments will be described in detail with reference to the accompanying drawings.

[0025] FIG. **1** is a block diagram showing an organic light-emitting diode (OLED) display device according to an exemplary embodiment of the present disclosure.

[0026] Referring to FIG. **1**, the OLED display device according to an exemplary embodiment of the present disclosure may include a display panel **100**, a scan driver **200**, a data driver **300**, and a timing controller **400**.

[0027] The display panel **100** displays images thereon. The display panel **100** may be connected to the scan driver **200** via first to n^{th} scan lines SL**1** to SLn, where n is a natural number equal to or greater than two. In addition, the display panel **100** may be connected to the data driver **300** via first to m^{th} data lines DL**1** to DLm, where m is a natural number equal to or greater than two. The display panel **100** may include a plurality of pixels PX. According to an exemplary embodiment of the present disclosure, the plurality of pixels PX may be electrically connected to the first to n^{th} scan lines SL**1** to SLn and the first to m^{th} data lines DL**1** to DLm, respectively.

[0028] The first to n^{th} scan lines SL**1** to SLn may be extended in a first direction d**1**. In addition, the first to m^{th} data lines DL**1** to DLm may be extended in a second direction d**2**. In an exemplary embodiment, the first direction d**1** may intersect the second direction d**2**. In FIG. **1**, the first direction d**1** refers to the row direction, and the second direction d**2** refers to the column direction. In an exemplary embodiment, the plurality of pixels may be arranged on a single substrate and may be insulated from one another, and may be arranged in a matrix.

[0029] The scan driver **200** may receive a first control signal CONT**1** from the timing controller **400**. The scan driver **200** may provide the first to the n^{th} scan signals SS**1** to SSn to the display panel **100** in response to the received first control signal CONT**1**.

[0030] In an exemplary embodiment, the data driver **300** may include a shift register, a latch, a digital-to-analog converter (DAC), etc. The data driver **300** may receive a second control signal CONT**2** and image data DATA from the timing controller **400**. The data driver **300** may select a reference voltage in response to the first control signal CONT**1**, and may convert the received image data DATA in the form of a digital wave into first to m^{th} data signals DS**1** to DSm based on the selected reference voltage. The data driver **300** may provide the generated data signals DS**1** to DSm to the display panel **100**.

[0031] The timing controller **400** may receive image signals R, G and B, and a control signal CS from an external device. In an exemplary embodiment, the control signal CS may include a vertical synchronous signal, a horizontal synchronous signal, a main clock signal, a data enable signal, etc. The timing controller **400** may process the signals received from an external device so that they are suitable for the operating conditions of the display panel **100**, and then may generate the image data DATA, the first control signal CONT**1**, and the second control signal CONT**2**.

[0032] The first control signal CONT**1** may include a scan start signal to instruct to start outputting the first to n^{th} gate signals SS**1** to SSn, and a gate clock signal for controlling the output timing of scan-on-pulses, etc. The second control signal CONT**2** may include a horizontal synchronous start signal to instruct to start inputting the image data DADA and a load signal for controlling application of the first to m^{th} data signals DS**1** to DSm to the first to m^{th} data lines DL**1** to DLm, respectively, etc.

[0033] Although not shown in the drawings, the OLED device according to an exemplary embodiment of the present disclosure may further include a power supplier. The power supplier may supply a first driving voltage ELVDD and a second driving voltage ELVSS to the plurality of pixels according to the control signal received from the

timing controller **400**. The potential of the first driving voltage ELVDD is higher than the potential of the second driving voltage ELVSS.

[0034] FIG. **2** is an equivalent circuit diagram schematically showing one pixel PX from FIG. **1**. In FIG. **2**, the pixel PX electrically connected to the first scan line SL**1** and the first data line DL**1** will be described.

[0035] Referring to FIG. **2**, the pixel PX may include a first switching device TR**1**, a second switching device TR**2**, an organic light-emitting diode OLED, and a storage capacitor Cst.

[0036] The first switching device TR**1** may be electrically connected to the first scan line SL**1**, the first data line DL**1**, and the second switching device TR**2**. In an exemplary embodiment, the first switching device TR**1** and the second switching device TR**2** may be three-terminal devices, e.g., thin-film transistors. In the following description, it is assumed that the first switching device TR**1** and the second switching device TR**2** are thin-film transistors.

[0037] The first switching device TR**1** may include a control electrode electrically connected to the first scan line SL**1**, a first electrode electrically connected to the first data line DL**1**, and a second electrode electrically connected to the control electrode of the second switching device TR**2**.

[0038] The second switching device TR**2** may include a control electrode electrically connected to the second electrode of the first switching device TR**1**, a first electrode electrically connected to a driving voltage line ELVDDL (see FIG. **3**) supplied to a first driving voltage ELVDD, and a second electrode electrically connected to the organic light-emitting diode OLED.

[0039] A first electrode of the storage capacitor Cst may be electrically connected to the second electrode of the first switching device TR**1**, and a second electrode of the storage capacitor Cst may be electrically connected to the driving voltage line ELVDDL (see FIG. **3**) via which the first driving voltage ELVDD is supplied.

[0040] The first switching device TR**1** may be turned on in response to the scan signal supplied from the first scan line SL**1**, and may provide the data signal supplied from the first data line DL**1** to the storage capacitor Cst. The storage capacitor Cst may be charged with voltage equal to the difference between the voltage of the received data signal and the first driving voltage ELVDD. The second switching device TR**2** can control the amount of the driving current supplied to the organic light-emitting diode OLED according to the voltage charged in the storage capacitor Cst. That is, the first switching device TR**1** may be a switching transistor, and the second switching device TR**2** may be a driving transistor.

[0041] It is to be noted that the first switching device TR**1** and the second switching device TR**2** may be formed as a single stacked switching device. More detailed description thereof will be made with reference to FIGS. **3** to **7**. Descriptions will be made focusing on the substrate on which the stacked switching device is disposed.

[0042] FIG. **3** is a layout diagram schematically showing a top view of the pixel PX. FIG. **4** is a view of a first gate conductor among the elements of the pixel PX, FIG. **5** is a view of a semiconductor pattern and a second gate electrode among the elements of the pixel PX, and FIG. **6** is a view of a data conductor among the elements of the pixel PX. FIG. **7** is a cross-sectional view along line I-I' in FIG. **3**, and FIG. **8** is a cross-sectional view along line II-II' in FIG. **3**.

[0043] Referring to FIGS. **3** to **8**, the substrate **110** may be, e.g., an insulative substrate. The substrate **110** may include, e.g., a glass substrate, a quartz substrate, a ceramic substrate, or a plastic substrate. In another exemplary embodiment, the substrate **110** may be a flexible substrate that can be bent, folded, or rolled. Such a substrate **110** may include, but is not limited to, polyimide.

[0044] A buffer layer **120** may be disposed on the substrate **110**. The buffer layer **120** may prevent permeation of impurity elements and may provide a flat surface. In an exemplary embodiment, the buffer layer **120** may include one of, e.g., a silicon nitride (SiN_x) layer, a silicon oxide (SiO_2) layer, and a silicon oxynitride (SiO_xN_y) layer. The buffer layer **120** may be eliminated depending on the type of the substrate **110**, process conditions, etc.

[0045] Referring to FIG. **4**, a first gate conductor GW**1** may be disposed on the buffer layer **120**. The first gate conductor GW**1** may include a plurality of scan lines including the first scan line SL**1** and a first gate electrode GE**1**. The first gate electrode GE**1** may be extended from the first scan line SL**1** and may be disposed on the same layer as the first scan line SL**1** to be electrically connected to the first scan line SL**1**. However, this is merely illustrative. The first gate electrode GE**1** and the first scan line SL**1** may be disposed on different layers. When the first gate electrode GE**1** and the first scan line SL**1** are disposed on different layers, they may be electrically connected to each other through an additional contact hole.

[0046] As illustrated in FIGS. **7-8**, the first gate electrode GE**1** of the first gate conductor GW**1** may at least partially overlap with a semiconductor pattern ACT to be described later. In an exemplary embodiment, the first gate conductor GW**1** may include at least one of an aluminum (Al)-based metal including an aluminum alloy, a silver (Ag)-based metal including a silver alloy, a copper (Cu)-based metal including a copper alloy, a molybdenum (Mo)-based metal including a molybdenum alloy, chromium (Cr), titanium (Ti), and tantalum (Ta). That is, the first gate electrode GE**1** and the first scan line SL**1** may be formed simultaneously via the same mask process. It is to be understood that the shape of the first gate electrode GE**1** is not necessarily limited to that shown in FIG. **3**.

[0047] As illustrated in FIGS. **7-8**, a first insulating layer **130** may be disposed on the first gate conductor GW**1**. The first insulating layer **130** may be made of at least one of an inorganic insulating material, e.g., silicon oxide (SiO_x) and silicon nitride (SiN_x), BCB (BenzoCycloButene), an acryl-based material, and an organic insulating material, e.g., polyimide, or a mixture thereof. That is, in an exemplary embodiment, the first insulating layer **130** may be a gate insulator.

[0048] The semiconductor pattern ACT may be disposed on the first insulating layer **130**. At least a part of the semiconductor pattern ACT may overlap with the first gate electrode GE**1**. Further, at least a part of the semiconductor pattern ACT may overlap with a second gate electrode GE**2**, which will be described later. As used herein, the phrase "two elements overlap with one another" means that the two elements overlap with one another in the vertical direction with respect to the substrate **110**. That is, the semiconductor pattern ACT may be disposed between the first gate electrode GE**1** and the second gate electrode GE**2**.

[0049] In an exemplary embodiment, the semiconductor pattern ACT may be made of at least one of, e.g., amorphous

silicon, polycrystalline silicon, single crystal silicon, and low-temperature polycrystalline silicon or a mixture thereof. In another exemplary embodiment, the semiconductor pattern ACT may include an oxide semiconductor.

[0050] The semiconductor pattern ACT may include a first source region Si, a first drain region D**1**, a second source region S**2**, and a second drain region D**2** (FIG. **5**). The first source region S**1** is defined as a portion of the semiconductor pattern ACT that is electrically connected to the first data line DL**1** through the first contact hole CNT**1**, and the first drain region D**1** is defined as a portion of the semiconductor pattern ACT that is electrically connected to the second gate electrode GE**2** through the second contact hole CNT**2** (FIG. **7**). The second source region S**2** is defined as a portion of the semiconductor pattern ACT that is electrically connected to the driving voltage line ELVDDL through the third contact hole CNT**3**, and the second region D**2** is defined as a portion of the semiconductor pattern ACT that is electrically connected to the connecting electrode CE and the pixel electrode PE through the fourth contact hole CNT**4** (FIG. **8**).

[0051] The second insulating layer **140** may be disposed on the semiconductor pattern ACT. The second insulating layer **140** may be made of at least one of an inorganic insulating material, e.g., silicon oxide (SiO_x) and silicon nitride (SiN_x), BCB (BenzoCycloButene), an acryl-based material, and an organic insulating material, e.g., polyimide, or a mixture thereof.

[0052] The second gate electrode GE**2** may be disposed on the second insulating layer **140**. The second gate electrode GE**2** may at least partially overlap with the semiconductor pattern ACT. For example, as illustrated in FIGS. **3** and **7**, the semiconductor pattern ACT may be between the first and second gate electrodes GE**1** and GE**2**, and the semiconductor pattern ACT with the first and second gate electrodes GE**1** and GE**2** may at least partially overlap each other. For example, as illustrated in FIGS. **3** and **7**, the first and second gate electrodes GE**1** and GE**2** may be stacked on top of each other with the semiconductor pattern ACT therebetween, such that different portions of the semiconductor pattern ACT may function as source and drain regions of each of the first and second gate electrodes GE**1** and GE**2**. For example, the second gate conductor GE**2** may include at least one of an aluminum (Al)-based metal including an aluminum alloy, a silver (Ag)-based metal including a silver alloy, a copper (Cu)-based metal including a copper alloy, a molybdenum (Mo)-based metal including molybdenum alloy, chromium (Cr), titanium (Ti), and tantalum (Ta).

[0053] The second gate electrode GE**2** may be electrically connected to the semiconductor pattern ACT. In an exemplary embodiment, the second gate electrode GE**2** may be electrically connected to the semiconductor pattern ACT through the second contact hole CNT**2** (e.g., FIGS. **3** and **7**). The second gate electrode GE**2** is one of the elements of the second switching device TR**2**. That is, the second gate electrode GE**2** may be directly electrically connected to the first drain region D**1** of the semiconductor pattern ACT through the second contact hole CNT**2**. Therefore, the first switching device TRI may be directly connected to the second gate electrode GE**2** through the first drain region D**1** in the semiconductor pattern ACT without forming an additional drain electrode, e.g., without requiring a separate drain electrode.

[0054] Accordingly, the second gate electrode GE**2** may receive the data signal from the first data line DL**1** through the switching operation of the first switching device TR**1**. In addition, the second gate electrode GE**2** overlaps with the third gate electrode GE**3**, which will be described later, to form the storage capacitor Cst.

[0055] The third insulating layer **150** may be disposed on the second gate electrode GE**2**. The third insulating layer **150** may be made of at least one of an inorganic insulating material, e.g., silicon oxide (SiO_x) and silicon nitride (SiN_x), BCB (BenzoCycloButene), an acryl-based material, and an organic insulating material, e.g., e.g., polyimide, or a mixture thereof.

[0056] The third gate electrode GE**3** may be disposed on the third insulating layer **150**. The third gate electrode GE**3** may at least partially overlap with the second gate electrode GE**2**. For example, the third gate conductor GE**3** may include at least one of an aluminum (Al)-based metal including an aluminum alloy, a silver (Ag)-based metal including a silver alloy, a copper (Cu)-based metal including a copper alloy, a molybdenum (Mo)-based metal including molybdenum alloy, chromium (Cr), titanium (Ti), and tantalum (Ta).

[0057] The third gate electrode GE**3** may be electrically connected to the driving voltage line ELVDDL, which will be described later, through a sixth contact hole CNT**6**. That is, the third gate electrode GE**3** may receive the first driving voltage ELVDD from the driving voltage line ELVDDL. As described above, the third gate electrode GE**3** may form the storage capacitor Cst together with the second gate electrode GE**2**. Accordingly, the storage capacitor Cst may be charged with voltage equal to the voltage difference between the data signal provided to the second gate electrode GE**2** and the first driving voltage ELVDD provided to the third gate electrode GE**3**.

[0058] The fourth insulating layer **160** may be disposed on the third gate electrode GE**3**. The fourth insulating layer **160** may be made of at least one of an inorganic insulating material, e.g., silicon oxide (SiO_x) and silicon nitride (SiN_x), BCB (BenzoCycloButene), an acryl-based material, and an organic insulating material, e.g., polyimide, or a mixture thereof. If the gate electrode GE**3** is eliminated, the fourth insulating layer **160** may also be eliminated.

[0059] Referring to FIGS. **6-8**, the data conductor DW may be disposed on the fourth insulating layer **160**. The data conductor DW may include the first data line DL**1**, the driving voltage line ELVDDL, and a connecting electrode CE. In an exemplary embodiment, the data line DW may have a single-layer structure or a multi-layers structure made of, e.g., nickel (Ni), cobalt (Co), titan (Ti), silver (Ag), copper (Cu), molybdenum (Mo), aluminum (Al), beryllium (Be), niobium (Nb), gold (Au), iron (Fe), selenium (Se), tantalum (Ta), etc. In addition, an alloy formed by adding at least one element of, e.g., titanium (Ti), zirconium (Zr), tungsten (W), tantalum (Ta), niobium (Nb), platinum (Pt), hafnium (Hf), oxygen (O) and nitrogen (N), to the metal may be used as the material of the data conductor DW.

[0060] The source electrode of the first switching device TR**1** may be electrically connected to the first data line DL**1**. That is, the source electrode of the first switching device TR**1** and the first data line DL**1** may be a single piece. The source electrode of the second switching device TR**2** may be electrically connected to the driving voltage line ELVDDL. That is, the source electrode of the second switching device TR**2** and the driving voltage line ELVDDL may be a single piece.

[0061] As described above, a drain electrode of the first switching device TR**1** is not additionally formed, and the first drain region D**1** of the semiconductor pattern ACT may be directly connected to the second gate electrode GE**2** of the second switching device TR**2**.

[0062] The drain electrode of the second switching device TR**2** and the connecting electrode CE may be a single piece. The connecting electrode CE may be directly connected to the second drain region D**2** of the semiconductor pattern ACT through the fourth contact hole CNT**4**.

[0063] A planarization layer **170** may be disposed on the data conductor DW. In an exemplary embodiment, the planarization layer **170** may include an organic material. For example, the planarization layer **170** may include at least one of polyimide, polyacryl, and polysiloxane. A fifth contact hole CNT**5** may be formed in the planarization layer **170** to expose at least a part of the connecting electrode CE.

[0064] The pixel electrode PE may be disposed on the planarization layer **170**. The pixel electrode PE may be electrically connected to the connecting electrode CE exposed via the fifth contact hole CNT**5**. The connecting electrode CE is electrically connected to the second drain region D**2** of the semiconductor pattern ACT exposed via the fourth contact hole CNT**4**, and in turn the pixel electrode PE is electrically connected to the second drain region D**2** of the semiconductor pattern ACT. The pixel electrode PE may be an anode which is a hole injection electrode. In an exemplary embodiment, the pixel electrode PE may be made of a transparent conductive material, e.g., ITO and IZO or a reflective metal, e.g., aluminum, silver, chrome or an alloy thereof. A pixel defining layer, an organic emitting layer, and a common electrode may be further disposed on the pixel electrode PE.

[0065] Accordingly, the data signal provided through the first data line DL**1** may be provided to the second gate electrode GE**2** of the second switching device TR**2** through the switching operation of the first switching device TR**1**. The second gate electrode GE**2** corresponds to one electrode of the storage capacitor Cst. The third gate electrode GE**3** receiving the first driving voltage ELVDD from the driving voltage line ELVDDL corresponds to the other electrode of the storage capacitor Cst. Accordingly, the storage capacitor Cst may be charged with voltage equal to the voltage difference between the data signal provided to the second gate electrode GE**2** and the first driving voltage ELVDD provided to the third gate electrode GE**3**. The second switching device TR**2** may perform switching operation according to the voltage charged in the storage capacitor Cst to adjust the amount of the driving current flowing from the driving voltage line ELVDDL to the pixel electrode PE.

[0066] By way of summation and review, aspects of the present disclosure provide an

[0067] OLED display device capable of achieving high integration by including a stacked switching device. That is, the first switching device TR**1** and the second switching device TR**2** may operate as a single stacked switching device. By doing so, an area occupied by the switching device in one pixel can be reduced, thereby achieving high integration.

[0068] In the foregoing description, the first switching device TR**1** and the second switching device TR**2** are PMOS transistors. However, it is to be understood that the first switching device TR**1** and the second switching device TR**2** may be implemented as NMOS or CMOS transistors depending on impurities doped in the semiconductor pattern ACT.

[0069] Example embodiments have been disclosed herein, and although specific terms are employed, they are used and are to be interpreted in a generic and descriptive sense only and not for purpose of limitation. In some instances, as would be apparent to one of ordinary skill in the art as of the filing of the present application, features, characteristics, and/or elements described in connection with a particular embodiment may be used singly or in combination with features, characteristics, and/or elements described in connection with other embodiments unless otherwise specifically indicated. Accordingly, it will be understood by those of skill in the art that various changes in form and details may be made without departing from the spirit and scope of the present invention as set forth in the following claims.

What is claimed is:

1. An organic light-emitting diode (OLED) display device, comprising:

a substrate;

a first gate electrode disposed on the substrate;

a second gate electrode disposed on the first gate electrode and at least partially overlapping the first gate electrode;

a semiconductor pattern disposed between the first gate electrode and the second gate electrode and at least partially overlapping the first and second gate electrodes;

a connecting electrode disposed on the second gate electrode and electrically connected to the semiconductor pattern; and

a pixel electrode disposed on the connecting electrode and electrically connected to the connecting electrode.

2. The OLED display device as claimed in claim **1**, wherein the second gate electrode is directly connected to the semiconductor pattern.

3. The OLED display device as claimed in claim **1**, wherein the connecting electrode is directly connected to the semiconductor pattern, and the pixel electrode is directly connected to the connecting electrode.

4. The OLED display device as claimed in claim **1**, further comprising:

a third gate electrode disposed between the second gate electrode and the connecting electrode; and

a driving voltage line disposed on a same layer as the connecting electrode and electrically connected to the third gate electrode.

5. The OLED display device as claimed in claim **1**, wherein the connecting electrode overlaps with the pixel electrode.

6. The OLED display device as claimed in claim **1**, wherein the semiconductor pattern includes an oxide semiconductor.

7. The OLED display device as claimed in claim **1**, further comprising a first scan line extended in a first direction, and a first data line extended in a second direction intersecting the first direction.

8. The OLED display device as claimed in claim **7**, wherein:

the semiconductor pattern includes a first source region, a first drain region opposed to the first source region in

the first direction, a second source region, and a second drain region opposed to the second source region in the second direction, and

the first data line is electrically connected to the first source region, the second gate electrode is electrically connected to the first drain region, and the connecting electrode is electrically connected to the second drain region.

9. The OLED display device as claimed in claim **8**, further comprising a driving voltage line extended in the second direction and disposed on a same layer as the first data line, the driving voltage line being electrically connected to the second source region.

10. An organic light-emitting display (OLED) display device, comprising:

a substrate;

a first gate electrode disposed on the substrate;

a semiconductor pattern disposed on the first gate electrode and including a first source region, a second source region, a first drain region, and a second drain region;

a second gate electrode disposed on the semiconductor pattern and electrically connected to the first drain region of the semiconductor pattern;

a connecting electrode disposed on the second gate electrode and electrically connected to the second drain region of the semiconductor pattern;

a data line disposed on a same layer as the connecting electrode and electrically connected to the first source region; and

a driving voltage line disposed on a same layer as the data line and electrically connected to the second source region.

11. The OLED display device as claimed in claim **10**, further comprising a pixel electrode disposed on the connecting electrode, the pixel electrode being electrically connected to the connecting electrode.

12. The OLED display device as claimed in claim **11**, wherein the pixel electrode at least partially overlaps with the connecting electrode.

13. The OLED display device as claimed in claim **10**, wherein the second gate electrode is directly connected to the first drain region, and the connecting electrode is directly connected to the second drain region.

14. The OLED display device as claimed in claim **10**, further comprising a third gate electrode disposed between the connecting electrode and the second gate electrode, the third gate electrode being electrically connected to the driving voltage line.

15. The OLED display device as claimed in claim **10**, wherein the semiconductor pattern includes an oxide semiconductor.

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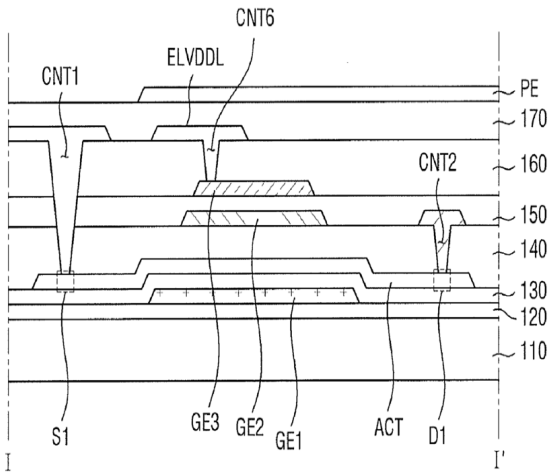
一种有机发光二极管（OLED）显示装置，包括基板，基板上的第一栅电极，第一栅电极上的第二栅电极，并且至少部分地与第一栅电极重叠，第一栅电极之间的半导体图案第二栅电极至少部分地与第一和第二栅电极重叠，第二栅电极上的连接电极与半导体图案电连接，连接电极上的像素电极与连接电极电连接。